

Abstract of the Disclosure**Software Implementation of Synchronous Memory Barriers**

5 Selectively emulating sequential consistency in software improves efficiency in a
multiprocessing computing environment. A writing CPU uses a high priority inter-processor
interrupt to force each CPU in the system to execute a memory barrier. This step invalidates old
data in the system. Each CPU that has executed a memory barrier instruction registers completion
and sends an indicator to a memory location to indicate completion of the memory barrier
instruction. Prior to updating the data, the writing CPU must check the register to ensure
completion of the memory barrier execution by each CPU. The register may be in the form of an
array, a bitmask, or a combining tree, or a comparable structure. This step ensures that all
invalidates are removed from the system and that deadlock between two competing CPUs is
avoided. Following validation that each CPU has executed the memory barrier instruction, the
writing CPU may update the pointer to the data structure.